

WHAT IS CLAIMED IS:

- 1 1. A method for performing timing analysis on a user design that has
2 been placed on a programmable integrated circuit, the method comprising:
3 generating edge masks to annotate edges in a graph that represents at least a
4 portion of the user design, the edge masks indicating whether a source or destination point is
5 reachable from a corresponding one of the edges; and
6 performing at least one depth first search along a time critical path in the graph
7 between the source and the destination points, the at least one depth first search being
8 prevented by the edge masks from analyzing paths that do not lead to the source point or the
9 destination point.
- 1 2. The method of claim 1 further comprising:
2 calculating slack and slack ratio values for edges in the time critical paths; and
3 if delay along any of the time critical paths exceeds the user timing constraint,
4 modifying placement of the user design within the programmable integrated circuit using the
5 slack and the slack ratio values.
- 1 3. The method of claim 2 wherein generating the edges masks further
2 comprises generating a first type of edge mask that represents reachability from the source
3 points in a backwards direction, and a second type of edge mask that represents reachability
4 to the destination points in a forward direction.
- 1 4. The method of claim 3 wherein generating the edge masks further
2 comprises generating binary bits that correspond to specific types of the source points and the
3 destination points in a list of constraints.
- 1 5. The method of claim 4 wherein performing the at least one depth first
2 search further comprises performing multiple depths first searches in the presence of multiple
3 constraints on timing analysis, wherein source edge-masks correspond to source-types in
4 timing constraints and source types correspond to source edge-masks.
- 1 6. The method of claim 5 further comprising:
2 converting multicycle constraints on timing analysis to two edge-mask sets,
3 one for a base case and another for a multicycle case.

1 7. The method of claim 5 further comprising:
2 converting thru-x constraints into multiple edge-mask sets indicating a base
3 case and a multicycle case, the multicycle case by masking out edges immediately adjacent to
4 node x in the base case.

1 8. The method of claim 6 wherein cut-path constraints on timing analysis
2 are treated as multicycle constraints with an infinite multicycle period.

1 9. The method of claim 4 wherein the resulting timing analysis is used in
2 combination with a placement algorithm to effect a modified placement of critical edges.

1 10. The method of claim 4 wherein generating the edge mask further
2 comprises generating source-edge-masks by depth-first search from destination registers or
3 pins in which edge-masks on a node or edge are defined as the inclusive OR of the edge
4 masks of their fanin edges or nodes.

1 11. The method of claim 4 wherein generating the edge masks further
2 comprises generating destination-edge-masks by depth-first search from source registers or
3 pins in which edge-masks on a node or edge are defined as the inclusive OR of the edge
4 masks of their fanout edges or nodes.

1 12. The method of claim 4 wherein generating the edge masks further
2 comprises generating one or more super-edge masks that are used to represent multiple
3 constraint types merged into a single constraint.

1 13. The method of claim 9 wherein generating the edge masks further
2 comprises generating additional edge masks to represent critical and non-critical portions of a
3 netlist for the user design, and the method further comprises:

4 applying timing analysis on the critical portion of the netlist with greater
5 frequency; and

6 applying timing analysis on the non-critical portion of the netlist less
7 frequently.

1 14. The method of claim 9 wherein the edge masks are used to identify
2 constraint domains in which placement changes are made, counters are made of the number

3 of constraint domains, and placement requests timing analysis only on the constraint domains
4 that have changed as the result of placement.

1 15. The method of claim 3 further comprising:
2 annotating the graph with a number of paths that pass each of the edges; and
3 successively pruning each edge, by setting the edge masks, until only k paths
4 remain to be reported to a user of a timing analysis tool.

1 16. The method of claim 15 wherein information reported to the user is a
2 set of k most critical paths within each constraint domain, reported separately.

1 17. The method of claim 16 wherein the number, k, is different for each
2 constraint domain.

1 18. A computer system for implementing timing analysis on a user design
2 that has been placed on a programmable integrated circuit, the computer system comprising:
3 code for generating edge masks to annotate edges in a graph that represents at
4 least a portion of the user design, the edge masks indicating whether a source point and a
5 destination point are reachable from a corresponding one of the edges;
6 code for performing at least one depth first search along a time critical path in
7 the graph between the source point and the destination point, the at least one depth first
8 search being prevented by the edge masks from analyzing paths that do not connect the
9 source and the destination points; and
10 a computer readable medium that stores the codes.

1 19. The computer system according to claim 18 further comprising:
2 code for calculating slack and slack ratio values for edges in the time critical
3 paths; and
4 code for modifying placement of the user design within the programmable
5 integrated circuit using the slack and the slack ratio values, if delay along any of the time
6 critical paths exceeds the user timing constraint.

1 20. The computer system according to claim 19 wherein the code for
2 generating the edges masks further comprises code for generating a first type of edge mask
3 that represents reachability from the source points in a backwards direction, and a second
4 type of edge mask that represents reachability to the destination points in a forward direction.

1 21. The computer system according to claim 20 wherein the code for
2 generating the edge masks further comprises code for generating binary bits that correspond
3 to specific types of the source points and the destination points in a list of constraints.

1 22. The computer system according to claim 21 wherein the code for
2 performing the at least one depth first search further comprises code for performing multiple
3 depths first searches in the presence of multiple constraints on timing analysis, wherein
4 source edge-masks correspond to source-types in timing constraints.

1 23. The computer system according to claim 22 further comprising:
2 code for converting multicycle constraints on timing analysis to two edge-
3 mask sets, one for a base case and another for a multicycle case.

1 24. The computer system according to claim 22 further comprising:
2 code for converting thru-x constraints into multiple edge-mask sets indicating
3 a base case and a multicycle case, the multicycle case by masking out edges immediately
4 adjacent to node x in the base case.

1 25. The computer system according to claim 23 wherein cut-path
2 constraints on timing analysis are treated as multicycle constraints with an infinite multicycle
3 period.

1 26. The computer system according to claim 21 wherein the code for
2 generating the edge mask further comprises code for generating source-edge-masks by depth-
3 first search from destination registers or pins in which edge-masks on a node or edge are
4 defined as the inclusive OR of the edge masks of their fanin edges or nodes.

1 27. The computer system according to claim 21 wherein the code for
2 generating the edge mask further comprises code for generating destination-edge-masks by
3 depth-first search from source registers or pins in which edge-masks on a node or edge are
4 defined as the inclusive OR of the edge masks of their fanout edges or nodes.

1 28. The computer system according to claim 21 wherein the code for
2 generating the edge masks further comprises code for generating one or more super-edge
3 masks that are used to represent multiple constraint types merged into a single constraint.

1 29. The computer system according to claim 21 wherein the code for
2 generating the edge masks further comprises code for generating edge masks to represent
3 critical and non-critical portions of a netlist for the user design, and the computer system
4 further comprises:

5 code for applying timing analysis on the critical portion of the netlist with
6 greater frequency; and

7 code for applying timing analysis on the non-critical portion of the netlist less
8 frequently.

1 30. The computer system according to claim 21 wherein the edge masks
2 are used to identify constraint domains in which placement changes are made, counters are
3 made of the number of constraint domains, and placement requests timing analysis only on
4 the constraint domains that have changed as the result of placement.

1 31. The computer system according to claim 20 further comprising:
2 code for annotating the graph with a number of paths that pass each of the
3 edges; and

4 code for successively pruning each edge, by setting the edge masks, until only
5 k paths remain to be reported to a user of a timing analysis tool.